**PATENTS** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Christos J. Georgiou, et al.

**Docket:** FIS920030113US1 (16497)

Serial No.:

10/604,491

Dated: . August 11,.2003

Filed: 07/25/03

For: SELF-CONTAINED PROCESSOR SUBSYSTEM

AS COMPONENT FOR SYSTEM-ON-CHIP DESIGN

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

## INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, applicants submit the following references which applicants believe may be material to the above-identified patent application. A copy of the references which applicants wish to make of record in this case is enclosed herein for the Examiner=s convenience along with a listing on Form PTO-1449 attached.

## CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is beir	ng deposited with the United States
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Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450 on	8/11/03

Dated: 8/11/03

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- 2. Nair, R., "Effect of increasing chip density on the evolution of computer architectures", IBM J. RES. & DEV., Vol. 46, No. 2/3, March/May 2002, pp. 223-234;
- 3. Ryu, et al., "A Comparison of Five Different Multi processor SoC Bus Architectures", Georgia Institute of Technology Electrical and Computer Engineering, Atlanta, GA;
- 4. Brinkman, et al., "On-Chip Interconnects for Next Generation System-on-Chips", <u>Heinz Nixdorf Institute and Department of Electrical Engineering</u>, <u>University of Paderborn, Germany, Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany</u>; and
- 5. Berry, "SYSTEM-ON-CHIP MARKETS AND TRENDS", <u>Electronic Trend Publications</u>, <u>Inc. San Jose</u>, <u>CA</u>, Second Edition, 2003, pp. 1-1 -5-2;

All the references listed on Form PTO-1449 are in the English language, thus, a concise explanation of those references required by 37 C.F.R. §1.98(a)(3) is not necessary.

Respectfully submitted,

Joseph P. Abate, Attorney Registration No. 30,238

Telephone No. (845)894-4633

International Business Machines Corporation Intellectual Property Law Department Zip 482 2070 Route 52 Hopewell Junction, NY 12533 Fax No. 845-892-6363

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EXAMINER DE LA CONTRACTOR DE LA CONTRACT		Title, Date, Pertinent Pages, Etc.)	
	Ryu, et al., "A Comparison f Five Different Mu Electrical and Computer Engineering, Atlanta, C	lti processor SoC Bus Architectures", G GA	eorgia Institute of Technology
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EXAMINER		DATE CONSIDERED	
*EXAMINER: Initi not considered. Inc	al if citation considered, whether or not citation is in conforn lude copy of this form with next communication to applicant.	nance with MPEP Section 609; Draw line the	rough citation if not in conformance and